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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,709	11/03/2003	Nicholas D. Signore	SUN-P9728-MEG	3521

28422 7590 10/06/2005

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/699,709	SIGNORE ET AL.	
	Examiner	Art Unit	TT
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-15 and 19-22* is/are rejected.

7)☒ Claim(s) *7-9 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 11/03/2003. Claims 1-22 are pending.

Information Disclosure Statement

1. The information disclosure statement filed on 12/22/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The crossed document listing in the Information Disclosure Statement (PTO-1449) has not been considered because it was not submitted. Also relevant pages of the document must be identified (see CFR 1.98(b)5).

Claim Objections

Claims 1, 10, and 19 are objected to because the " transistor fanout " and the " ratio of transistor sizes" are not clearly described in the specification. Examiner interprets they are the same meaning.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1, 10, and 19** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is: " Determine the Transistor Size from the Steady–State Solution" (see specification; page 10, lines 7-15; and Fig. 1, step 140) because it is a necessary step to determine an optimal transistor size from the steady-state solution in order to be able to perform the step " determining at least one transistor fanout from the steady state solution" recited in the claims.

4. **Claims 2-9, 11-18, and 20-22** are rejected because they depend on claim 1, 10, and 19.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-6, 10-15, and 19-22** are rejected under 35 U.S.C. 102(e) as being anticipated by Sutherland et al. (Sutherland)(US Patent No.6629301).

Referring to claim 1 and similarly recited claims 10 and 19, Sutherland discloses a method of determining at least one transistor fanout (one ratio of transistor size), the method comprising:

a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element (Fig. 6; col. 8, lines 55+) that includes a dynamic resistor (col. 3, lines 33-37; col. 9, lines 17-25; Sutherland discloses a sizing element includes a resistor which is tunable (i.e. " dynamic resistor"); Fig. 4-5, col. 7, lines);

b) determining a steady state solution to the sizing model (Fig. 6; col. 9, lines 1-6); and

c) determining at least one transistor fanout from the steady state solution (Fig. 6; col. 9, lines 1-6).

Referring to claim 2 and similarly recited claims 11 and 20, Sutherland discloses the method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current (col. 3, lines 1-20 and lines 44-55).

Referring to claim 3 and similarly recited claims 12 and 21, Sutherland discloses the method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a

dynamic resistor the size of which is based at least upon the logical effort of a logical element (col. 3, lines 1-20 and lines 44-55).

Referring to claim 4 and similarly recited claims 13 and 22, Sutherland discloses the method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage (col. 3, lines 1-20 and lines 44-55).

Referring to claim 5 **and similarly recited claim 14**, Sutherland discloses the method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current and a voltage (col. 3, lines 1-20 and lines 44-55).

Referring to claim 6 and similarly recited claim 15, Sutherland discloses the method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logic element, a current, and a voltage (col. 3, lines 1-20 and lines 44-55).

Allowable Subject Matter

7. **Claims 7- 9, and 16-18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. **Claims 7- 9, and 16-18** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claims 7 and 16)

a sizing element that includes a dynamic resistor the size of which is proportional to the square root of a current.

(Claims 8 and 17)

a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the logical effort of a logic.

(Claims 9 and 18)

a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the inverse of a voltage.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

VUTHE SIEK
PRIMARY EXAMINER